Confirmation No. 3872

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | GOFF | Examiner: | Mamo, E. |
| Serial No.: | 10/538,458 | Group Art Unit: | 2184 |
| Filed: | June 10, 2005 | Docket No.: | US020598US2 (NXPS.353PA) |
| Title: | ENCAPSULATED HARDWARE CONFIGURATION/CONTROL | | |

# APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Customer No.**
**65913**

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed August 24, 2009 and in response to the rejections of claims 1-15 as set forth in the Final Office Action dated May 29, 2009.

No fee is believed to be due for this filing, as the required fee was paid with a prior filing of an Appeal Brief dated September 23, 2008. If a fee is found to be necessary, please charge **Deposit Account 50-4019 (US020598US2)** the required fee.

## I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017413/0445 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

## II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

## III. Status of Claims

Claims 1-15 stand rejected and are presented for appeal. The final office action noted an objection to claims 7-10 due to informalities, which have been since been corrected. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

## IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated May 29, 2009.

## V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a method of performing configuration or control of a subsystem (*see, e.g.*, hardware subsystem 110 shown in Fig. 1, and page 2:23-26) that includes multiple registers that define multiple configurations of the subsystem (*see, e.g.*, registers 111 shown in Fig. 1, page 2:27-30, and page 3:1-7), comprising: providing together with the subsystem a configuration/control unit having a controller portion (*see, e.g.*, configuration/control state machine 113 shown in Fig. 1, and page 2:27-30) and a read-only storage portion storing multiple sets of configuration data (*see, e.g.*, read only memory 115 shown in Fig. 1, and page 2:27-30), each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and the configuration/control unit, in response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem (*see, e.g.*, page 3:1-7).

Commensurate with independent claim 6, an example embodiment of the present invention is directed to a subsystem having self-configuration capabilities (*see, e.g.*, hardware subsystem 110 shown in Fig. 1, and page 2:23-26), comprising: a register section including multiple registers that define multiple configurations of the subsystem (*see, e.g.*, registers 111 shown in Fig. 1, and page 2:27-30); and a configuration/control unit having a controller portion (*see, e.g.*, configuration/control state machine 113 shown in Fig. 1, and page 2:27-30) and a read-only storage portion storing multiple sets of configuration data (*see, e.g.*, read only memory 115 shown in Fig. 1, and page 2:27-30), each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; wherein the configuration/control unit is configured, responsive to a single register write that identifies one of the sets of configuration data, to encapsulate the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem (*see, e.g.*, page 3:1-7).

Commensurate with independent claim 11, an example embodiment of the present invention is directed to, for use in a system that includes a processor (*see, e.g.*, processor 101 shown in Fig. 1, and page 2:16-22) coupled to a hardware subsystem via a system bus (*see, e.g.*, system bus 103 shown in Fig. 1, and page 2:16-22), the hardware subsystem including a configuration/control unit (*see, e.g.*, configuration/control state machine 113 shown in Fig. 1, and page 2:27-30) and a plurality of registers (*see, e.g.*, registers 111 shown in Fig. 1, and page 2:27-30) that define multiple configurations of the subsystem, a method of configuring the subsystem comprising: storing a plurality of sets of configuration data in a read-only memory of the configuration/control unit (*see, e.g.*, read only memory 115 shown in Fig. 1, and page 2:27-30), each of the sets of configuration data including configuration parameters for each of the plurality of registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and responsive to the configuration/control unit receiving, from the processor, a single register write that identifies one of the sets of configuration data, encapsulating the plurality of registers by writing the configuration parameters of the identified set from the read-only memory to the plurality of registers (*see, e.g.*, page 3:1-7).

## VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-15 stand rejected under 35 U.S.C. § 103(a) over the Wu reference (U.S. Patent Pub. 2003/0041205).

## VII. Argument

### A. The § 103(A) Rejection Of Claims 1-15 Is Improper Because The Examiner Fails To Establish A *Prima Facie* Case Of Obviousness And Because The '205 Reference Teaches Away From The Examiner's Asserted Modification.

The § 103(a) rejection is improper because the '205 reference lacks correspondence to the claimed invention, as acknowledged by the Examiner. The claimed invention, in certain embodiments, is directed to enabling a system programmer to configure a hardware subsystem using a single register write. *See, e.g.,* page 1:9-23 of Appellant's specification. Appellant stores multiple sets of configuration data in a read-only memory of the hardware subsystem, thereby enabling the subsystem to be configured (or reconfigured) during operation by sending a single register write, to the subsystem, that identifies one of the sets of configuration data. *See, e.g.,* page 3:8-12 of Appellant's specification. The set of configuration data identified by the single register write is then loaded into multiple registers of the subsystem to configure the subsystem, thereby encapsulating the multiple registers. The Examiner acknowledges that the '205 reference does not teach such aspects of the claimed invention (*see* pages 3-4 of the Final Office Action dated May 29, 2009) and the Examiner fails to cite to any reference that does teach such aspects. Thus, the Examiner has failed to establish a *prima facie* case of obviousness due to the failure to cite a prior art reference that teaches each aspect of the claimed invention and the § 103(a) rejection must be reversed. Applicant submits that the Examiner appears to be improperly modifying the '205 reference in the manner taught only by Appellant's disclosure in an improper hindsight reconstruction of the claimed invention. *See, e.g.,* M.P.E.P. § 2142. The impropriety of the Examiner's proposed modification of the '205 reference is further highlighted by the Examiner's failure to provide a valid reason for the proposed modification and by the '205 reference teaching away from such a modification. The following discussion particularly addresses the impropriety of the § 103(a) rejection.

### 1. The § 103(A) Rejection Of Claims 1-15 Is Improper Because The '205 Reference Does Not Teach Encapsulating A Hardware Subsystem In Response To A Single Register Write.

The § 103(a) rejection is improper because the Examiner improperly concludes that aspects of the claimed invention are obvious without citing to any prior art reference that discloses such aspects. For example, the Examiner fails to cite a reference that teaches a configuration/control unit that, in response to a single register write that identifies one of the sets of configuration data, encapsulates the multiple registers, including storing the configuration parameters of the identified set in the multiple register, as in the claimed invention. The Examiner acknowledges that the '205 reference does not teach these aspects of the claimed invention and the Examiner fails to cite to any reference that does teach such aspects. Accordingly, the § 103(a) rejection necessary fails due to the Examiner's failure to cite to any reference that teaches or suggests encapsulating a subsystem in the manner of the claimed invention. Thus, Appellant respectfully submits that the § 103(a) rejection is improper and requests that it be withdrawn.

### 2. The § 103(A) Rejection Of Claims 1-15 Is Improper Because The '205 Reference Does Not Teach A Read-Only Storage Portion That Stores Multiple Sets Of Configuration Data.

The § 103(a) rejection is improper because the '205 reference does not teach a subsystem that includes a read-only storage portion that stores multiple sets of configuration data, as claimed. For example, the '205 reference does not teach that endpoint configuration mechanism 424 (*i.e.,* the asserted read-only storage portion) is a read-only memory that stores multiple sets of configuration data. Instead, the '205 reference teaches that configurations of each endpoint are stored in mechanism 424 to configure the device 40 during operation of the device 40. *See, e.g.,* Figure 4 and paragraph 0047. Thus, mechanism 424 is not a read-only storage portion because data is written to mechanism 424 during operation. In an apparent recognition of the lack of correspondence, the Examiner asserts that the skilled artisan would "store the configuration data in a type of memory ... suitable such as ROM, RAM and etc." *See* page 2 of the Advisory Action dated July 7, 2009. Thus, the Examiner has once again acknowledged the lack of correspondence. Moreover, while the

Examiner's hypothetical modification of mechanism 424 does not form the basis for the rejection under Appeal, Appellant submits that the skilled artisan would not modify the '205 reference to replace mechanism 424 with an ROM because such a modification would render the '205 reference inoperable since the '205 reference writes data to mechanism 424 during operation of the device. *See, e.g.,* M.P.E.P. § 2143.01.

In view of the above, Appellant respectfully submits that the § 103(a) rejection is improper and requests that it be withdrawn.

### 3. The § 103(a) Rejection Of Claims 1-15 Is Improper Because The Asserted Basis To Combine Is Contrary To The Requirements Of § 103 And Relevant Law.

The Examiner fails to provide a valid reason for the proposed modification of the '205 reference. "A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that the skilled artisan would modify the '205 reference to encapsulate the subsystem in the manner of the claimed invention because "such modification is merely an alternate arrangement". However, such a vague and hypothetical combination does not provide a clearly-articulated reason that would be consistent with *KSR*. Unlike *KSR*, where the combination involved combining "two known devices according to their established functions", the Examiner's proposed combination does not involve simply combining teachings in which the cited references are not modified in their operation.

More specifically, the '205 reference teaches that the configuration data of multiple endpoints 0, 1 and 2 are stored in memory buffer 440 (*see, e.g.,* paragraphs 0045-0047). The '205 reference does not teach and the Examiner has not provided any explanation regarding how the configuration of logic module 400 to interface with the multiple endpoints 0, 1 and 2 is to be accomplished in response to a single register write. As such, the Examiner's modification would necessarily involve (extensively) modifying the cited teachings of the '205 reference. Accordingly, the Examiner's assertion of some vague "articulated

reasoning" in support of the modification (*e.g.,* "an alternate arrangement" and "simplified operation") is insufficient. *KSR* and M.P.E.P. § 2141 make it clear that such assertions are inapplicable where the operation of one of the references is modified. For example, according to M.P.E.P. § 2141, Appellant can rebut such assertions of obviousness simply by showing that "the elements in combination do not merely perform the function that each element performs separately." This is also consistent with various parts of *KSR*, which repeatedly refer to combined teachings in which the cited references are not modified in their operation. As such, in the context of *KSR*, the asserted combination "as a whole" is entirely unpredictable based on the asserted teachings of the '205 reference.

In view of the above, Appellant respectfully submits that the § 103(a) rejection is improper and requests that it be withdrawn.

**4. In Attempting To Use An Obvious-To-Try Argument, The § 103 Rejection Contradicts Both The Patent Law And The Evidence That The '205 Reference Teaches Away From The Examiner's Asserted Modification.**

The '205 reference teaches away from encapsulating memory buffer 440 (*i.e.,* the asserted multiple registers) in response to a single register write, as claimed. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('205) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). In this instance, the '205 reference teaches that the configuration data of multiple endpoints 0, 1 and 2 are stored in memory buffer 440 (*see, e.g.,* paragraphs 0045-0047); as such, modifying the '205 reference to encapsulate memory buffer 440 in response to a single register write that indentifies one set of configuration data would render the device of the '262 reference unable to interface/control the multiple endpoints 0, 1 and 2. Thus, the '262 reference teaches away from such a modification.

Moreover, Appellant submits that the Examiner's assertion regarding modifying the '205 reference is based on an "obvious to try" assertion that contradicts one of the two situations, as explained in *In re Kubin*, in which the "obvious to try" standard may not be applied. *In re Kubin*, 561 F.3d 1351 (Fed. Cir. 2009). Specifically, the evidence of record does not indicate that the '205 reference provides any direction as to how the skilled artisan would modify the '205 reference to encapsulate memory buffer 440 in response to a single register write or that the '205 reference provides any direction as to which of many possible choices of performing such an encapsulation is likely to be successful. Without further explanation, the record indicates that, at best, the Examiner's assertions are based solely on "obvious to try" arguments. Such a rejection, however, has been reviewed and assessed adversely by the *In re Kubin* court which explains that the "obvious to try" standard may not be applied where one would have "to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful." *In re Kubin* (Fed. Cir. April 3, 2009), *interpreting KSR*. *See also* M.P.E.P. § 2143(E), and *Gillette Co. v. S.C. Johnson & Son, Inc.,* 919 F.2d 720, 725 (Fed. Cir. 1990) ("we have consistently held that 'obvious to try' is not to be equated with obviousness.").

In view of the above, Appellant respectfully submits that the § 103(a) rejection is improper and requests that it be withdrawn.

## VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-15 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account if necessary was provided on the first page of this brief.

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## APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,458)

1. A method of performing configuration or control of a subsystem that includes multiple registers that define multiple configurations of the subsystem, comprising:

providing together with the subsystem a configuration/control unit having a controller portion and a read-only storage portion storing multiple sets of configuration data, each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and

the configuration/control unit, in response to a single register write that identifies one of the sets of configuration data, encapsulating the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem.

2. The method of claim 1, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode, each of the modes encapsulated by a single write to a common register location, and wherein the subsystem is a hardware subsystem, and the configuration/control unit is a hardware configuration/control unit.

3. The method of claim 2, wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

4. The method of claim 1, wherein the storing of the configuration parameters of the identified set in the multiple registers is implemented using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set.

5. The method of claim 1, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding

configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.

6. A subsystem having self-configuration capabilities, comprising:

a register section including multiple registers that define multiple configurations of the subsystem; and

a configuration/control unit having a controller portion and a read-only storage portion storing multiple sets of configuration data, each of the sets of configuration data including configuration parameters for each of the multiple registers, and each of the sets of configuration data defining a respective one of the multiple configurations; wherein the configuration/control unit is configured, responsive to a single register write that identifies one of the sets of configuration data, to encapsulate the multiple registers by performing configuration or control of the subsystem, including storing the configuration parameters of the identified set in the multiple registers of the subsystem.

7. The subsystem of claim 6, wherein the subsystem is a universal serial bus (USB) block, and the multiple configurations include Control mode, Interrupt mode, Isochronous mode, and Bulk mode, each of the modes encapsulated by a single write to a common register location, and wherein subsystem is a hardware subsystem, and the configuration/control unit is a hardware configuration/control unit.

8. The subsystem of claim 7 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

9. The subsystem of claim 6, further comprising a bus having a width sufficient to simultaneously store the configuration parameters of the identified set in the multiple registers.

10. The subsystem of claim 6, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding

configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.

11. For use in a system that includes a processor coupled to a hardware subsystem via a system bus, the hardware subsystem including a configuration/control unit and a plurality of registers that define multiple configurations of the subsystem, a method of configuring the subsystem comprising:

storing a plurality of sets of configuration data in a read-only memory of the configuration/control unit, each of the sets of configuration data including configuration parameters for each of the plurality of registers, and each of the sets of configuration data defining a respective one of the multiple configurations; and

responsive to the configuration/control unit receiving, from the processor, a single register write that identifies one of the sets of configuration data, encapsulating the plurality of registers by writing the configuration parameters of the identified set from the read-only memory to the plurality of registers.

12. The method of claim 11, wherein the configuration/control unit is a state machine.

13. The method of claim 11, wherein the subsystem is a USB block comprising a plurality of ports that can operate in different modes responsive to which of the sets of configuration data is written to the plurality of registers.

14. The method of claim 11, wherein the storing of the configuration parameters of the identified set in the plurality of registers is implemented using a bus having a width sufficient to simultaneously store the configuration parameters of the identified set.

15. The method of claim 11, wherein the configuration/control unit is responsive to multiple different values for the single register write for performing different corresponding

configuration or control actions with respect to the subsystem, each of the different values identifying one of the sets of configuration data.

## APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

## APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.